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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,936	08/22/2003	Samuel D. Naffziger	200210023-1	3016

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EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	**PAPER NUMBER**
2817	

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,936	NAFFZIGER ET AL.	
	Examiner	Art Unit	
	Michael B. Shingleton	2817	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-27 and 30-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *2-11 and 30-32* is/are allowed.

6)☒ Claim(s) *12,13,16,17,21-24 and 26* is/are rejected.

7)☒ Claim(s) *14, 15,18-20, 25, 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 12, 13, 16, 17, 21-24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizokawa 4,170,715 (Mizokawa).

Figures 2 and 3 and the relevant text of Mizokawa discloses a clock generator having a driver 5 that provides an output clock signal "c" that is based on at least one control signal NRZ "a"; SPM "b" and the signal applied at the output of device 24. The examiner must give the broadest reasonable interpretation to the claims consistent with the specification (See MPEP 904.01 and 2111). The device of Mizokawa in producing a square wave like that shown in Figure 2 is fully capable as operating as a clock. A clock is in its simplest form merely a square wave generator. The waveform "c" is square wave. This then qualifies Mizokawa's circuit as a clock. A waveform controller is formed by the unshown device that produces the NRZ "a" signal, the SPM device that produces the SPM "b" signal and the device 24 that produces a control signal at its output. During the first operating mode the waveform controller of Mizokawa controls the driver 5 to provide the output clock signal having normally high and low levels. The first operating mode being defined by when the NRZ data "a" is at zero and the SPM data "b" is don't care i.e. either a 1 or a zero (See Figure 3). During the second operating mode the waveform controller or Mizokawa controls the driver 5 to provide temporarily the output signal at an intermediate level between the normally high and low levels. The second operating mode being defined by when the NRZ data "a" is a one and the SPM data "b" is don't care. As noted by Figure 3 of Mizokawa NRZ is only at the "one" level on a temporarily basis and thus it goes without saying that output signal is temporarily at an intermediate level between the normally high and low levels in Mizokawa. Note that when NRZ is a "one" then the transistor T conducts thus forming a voltage divider with the winding 5a wherein the node of the voltage divider, i.e. the center node of the winding 5a causes a reduced voltage at this node which in turn provides the clock signal at the intermediate level during this second operating mode as indicated in Figure 3 of Mizokawa. The transistor T being a bipolar conducts main current only in a single direction and thus meets the limitation of being a device that temporarily "diode connects" a device of the driver i.e. the winding 5a to enable the driver to provide the clock signal at the intermediate level during the second operating mode. Applicant has not provided a specific definition for the term

"self-biases" and as such the examiner must give the broadest reasonable interpretation to this term consistent with the specification. Thus a reasonable interpretation would be that the clock signal self-biases to the intermediate based on the relative characteristics of the driver, i.e. the voltage divider that is formed by the winding 5a and at least the transistor T. Note that the source that provides the signal a would be called a predriver. Mizokawa is silent on integrating the circuit arrangement, however, it is conventionally known to integrate a circuit so as to make for a more compact and reliable structure. Thus it would have been obvious to one of ordinary skill in the art to have integrated the structure of Mizokawa so as to provide for a more compact and reliable structure as is conventionally known in the art. Applicant claims that the output transitions from a high to an intermediate level and then to a low level or form a low to an intermediate level and then to a high level. This is dependent on the timing of the SPM data as compared to the NRZ signal of Mizokawa. Note that the output of Mizokawa can transition from an intermediate value to a low value and from an intermediate value to a high value. Thus Mizokawa would be fully capable of operating in the manner claimed. Thus the general condition of the claim is disclosed in the Mizokawa reference. As such, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have provided the transitions from a intermediate value to a low value and then back to an intermediate value to a high value as this is merely part of the operating range of the system, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105, USPQ 233. as this is merely part of the operation range of the circuit which

All the reasoning above as applied above and the following: In the waveform controller circuitry of Mizokawa there must be a delay network because the SPM data and the NRZ data have preset periods as is clearly apparent in Figure 3 of Mizokawa. However, it conventionally known to utilize a delay network so as to form a preset period in a square wave for example. It would have been obvious to one having ordinary skill in the art at the time the invention was made to have utilized a delay network to set the period for the control waveforms in Mizokawa wherein it is noted that the period of the control waveforms control the duration of the clock signal when it is at an intermediate level, because as the Mizokawa is silent on the device that causes the delay, i.e. sets the period, one of ordinary skill in the art would have been motivated to use any art-recognized equivalent delay device to set the period such as a conventional delay network. With respect to claim 26, Mizokawa is silent on the circuit being "integrated". Mizokawa clearly shows at least one circuit 9, 10, etc. that is driven by the output "c" of the clock generator. Integration is well known to be advantageous so as to make the circuit smaller, cheaper and more durable. Thus it would have been obvious to integrate at least part of the circuitry of Mizokawa

thereby forming "an integrated" circuit so as to provide for a more compact structure, a cheaper (less expensive) structure and a more durable structure. One of ordinary skill would have been motivated to make the combination so as to provide a smaller, cheaper and more durable structure. These are well known advantages to integrating a circuit.

Claims 14, 16, 18-20, 25 and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 2-11, 30 and 32 are allowable over the prior art of record.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is (571) 272-1770.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (571)272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306 and after July 15, 2005 the fax number will be 571-273-8300. Note that old fax number (703-872-9306) will be service until September 15, 2005.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MBS

December 09, 2005

Michael B Shingleton
Primary Examiner
Group Art Unit 2817